CLAIMS

1. A clock generation circuit, which selects one of a plurality of reference signals and generates a clock that is synchronized with a selected reference signal, the clock generation circuit comprising:

(1) a plurality of former stage PLL circuits respectively provided for each of the plurality of reference signals, generating outputs that are respectively synchronized with a corresponding reference signal;

(2) a selection circuit selecting one of the outputs from the plurality of former stage PLL circuits; and

(3) a latter stage PLL circuit linked in sequence to the plurality of former stage PLL circuits, for receiving the one of the outputs selected and generating the clock.

2. The clock generation circuit according to claim 1, further comprising a plurality of phase control circuits, respectively provided for each of the outputs from the plurality of former stage PLL circuits, for matching phase of an output from another one of the plurality of former stage PLL circuits with phase of an output from one of the plurality of former stage PLL circuits corresponding to the selected reference signal.

3. The clock generation circuit according to claim 2, wherein

the phase control circuits includes a ring counter and a selection circuit selecting one of multiphase outputs from the ring counter.

4. The clock generation circuit according to claim 1, wherein the plurality of former stage PLL circuits respectively perform synchronization in frequency with a corresponding reference signal, respectively, and

wherein the latter stage PLL circuit performs synchronization in phase with the selected reference signal,

the clock generation circuit further comprising,

a plurality of phase control circuits respectively provided for each of the outputs from the plurality of former stage PLL circuits,

wherein the clock generation circuit controls a phase control circuit corresponding to the selected reference signal such that phase of a signal obtained by dividing the generated clock matches phase of the selected reference signal, and

wherein the plurality of phase control circuits matchphase of an output from another one of the plurality of former stage PLL circuits with phase of an output from one of the plurality of former stage PLL circuits corresponding to the selected reference signal.

5. The clock generation circuit according to claim 4, wherein

the clock generation circuit controls the phase control circuit in commensurate with a cycle of the selected reference signal.

6. The clock generation circuit according to claim 4, wherein the clock generation circuit controls the phase control circuit in commensurate with a dividing cycle of the generated clock.